IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/043,974
Filed: October 19, 2001
Inventor:
Kane, et al.

Title: ERROR RECOVERY

§
§
§
§
§
§
§
§
§
§
§
§
§

Examiner: Manoskey, Joseph D
Group/Art Unit: 2113
Atty. Dkt. No: 5681-55600

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Stephen J. Curran
Name of Registered Representative

Signature

10/6/05
Date

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reason(s) stated below.

Claims 1-4, 10-13, 15, 19-21, and 24 are pending in the application. Reconsideration of the present case is earnestly requested in light of the following remarks. Please note that for brevity, only the primary arguments directed to the independent claims are presented, and that additional arguments, e.g., directed to the subject matter of the dependent claims, will be presented if and when the case proceeds to Appeal.

Claims 1-4, 10-13, 15, 19-21, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli et al. (U.S. Patent Number 6,480,975, hereinafter "Arimilli '975") in view of Arimilli et al. (U.S. Patent Number 5,867,511, hereinafter "Arimilli '511"). Applicant respectfully notes the following errors in the Examiner's rejection.

Regarding claim 1, Applicant submits that neither Arimilli '975 nor Arimilli '511, taken singly or in combination, teach or suggest "while the system is in operation: testing the at least a portion of the directory cache while the at least a portion of the directory cache is offline based on determining that the error is uncorrectable," nor "servicing the at least a portion of the directory cache in response to testing the directory cache," nor "dynamically placing the allowing access to the at least a portion of the directory cache in response to servicing the at least a portion of the directory cache" as recited in Applicant's claim 1. (Emphasis added).

The Examiner asserts, the combination of Arimilli '975 and Arimilli '511 teach Applicant's invention. More particularly, the Examiner acknowledges Arimilli '975 does not teach generating a cache miss in response to a request to access the directory cache. However, the Examiner asserts Arimilli '511 teaches this feature.

Applicant respectfully disagrees with the Examiner's characterization of Arimilli '975 and Arimilli '511 and his application of the cited art to Applicant's claims. Specifically, Arimilli '975 teaches at col. 6, lines 2 – 14,

> "This output is connected to a retry circuit 82 and an ECC circuit 84. Retry circuit 82 causes the cache operation to be repeated after a delay sufficient to allow ECC circuit 84 to complete its operation. ECC circuit 84 uses all of the bits from all address tags in congruence class 74, and further uses bits from a special ECC field 86. Only one ECC field is provided for each congruence class, rather than providing one ECC field for each cache block. When ECC circuit 84 operates on the input values, it

> generates corrected values which are fed back to the cache blocks and ECC field of the congruence class. If a double-bit error is detected, operation of **the processing unit can be halted** using an appropriate circuit 88." (Emphasis added)

From the foregoing, it appears Arimilli '975 teaches detecting and correcting certain classes of errors using a retry circuit and an ECC circuit, and if a certain uncorrectable classes of errors are detected, halting the processor. As such, in response to an error being detected by parity check circuits, the retry circuit may cause the request to occur again, this time the ECC circuit may correct the error is it is within the capabilities of the ECC circuit.

Thus, Applicant submits Arimilli '975 does not teach

> "while the system is in operation:
> ..., wherein making at least the portion of the directory cache unavailable comprises generating a cache miss in response to a request to access the directory cache;
> testing the at least a portion of the directory cache **while the at least a portion of the directory cache is offlin**e based on determining that the error is uncorrectable;
> servicing the at least a portion of the directory cache in response to testing the directory cache; and
> dynamically allowing access to the at least a portion of the directory cache in response to servicing the at least a portion of the directory cache.

In addition, Arimilli '511 teaches at col. 7, line 11 through col. 8, line 6

> "It can be seen that repair mask 76 is a convenient means for both keeping a defective cache line from **ever** indicating a cache hit and keeping a defective cache line from **ever** being chosen as a victim. ...
>
> This novel method of using functional masking to bypass defects in caches eliminates the performance degradation and the silicon area increase of the standard cache defect repair method. ...
>
> The use of a repair mask additionally allows for dynamic cache defect bypassing (of locations in the caches that are generating errors) by updating the repair mask real-time when the errors are detected. The cache

> lines may be tested initially at fabrication and any noted defects can be handled by permanently setting the value of the corresponding field in the repair mask. Thereafter, each time the computer is booted (turned on), the mask might be automatically updated based on firmware testing, as part of the boot process. Finally, the repair mask can be updated upon detection of directory parity errors, cache entry array ECC errors, or LRU errors. A hardware algorithm could be provided to set the values in the repair mask array. For example, one 2-bit field could be provided in the repair mask for each cache line. The 2-bit field may initially be set to zero, and incremented each time a error is detected on that cache line. This allows the 2-bit field to act as a counter, setting the cache line as defective only when three cumulative parity errors have been recorded for a given cache line.
>
> In order to continue to reliably run the processor after encountering defective cache locations, when the repair mask entry associated with the line in the cache is set to indicate the line is defective, the contents of the cache at that location are flushed. Once the repair mask entry has been set, **any future accesses** to that cache line will be forced by the repair mask to see a miss on that line, and the line would **never** be re-used (victimized). This solution has practically no overhead when compared to prior art schemes, such as redundant lines. It is also particularly useful in those applications where the processors operate in harsh environments but must continue to function in the event of run-time defects." (Emphasis added)

From the above, Arimilli '511 appears to teach overcoming cache defects within a processor by never again using the defective cache line and permanently causing a cache miss in response to an access request to a bad cache line by using a repair mask. The repair mask functionally bypasses accesses by "keeping a defective cache line from ever indicating a cache hit and keeping a defective cache line from ever being chosen as a victim." (*See* col. 7, lines 11-14) Arimilli '511 also teaches testing the cache during manufacturing and at boot-up and updating the repair mask as needed.

Applicant submits this is in contrast to Applicant's invention as claimed.

It is noted that the Examiner disagrees with Applicant in the Response to Arguments section of the Office action dated July 6, 2005. Specifically, the Examiner disagrees with Applicant's assertion that Arimilli teaches permanently causing a cache miss to an access to a bad cache line. In response, Applicant respectfully redirects the Examiner to col. 7 line 65 through col. 8, line 1, wherein Arimilli '511 discloses

> "Once the repair mask entry has been set, **any future accesses** to that cache line will be forced by the repair mask **to see a miss on that line**, and the line would **never** be re-used (victimized)." (Emphasis added)

In regard to the Examiner's assertion that the retry circuit allowing an ECC circuit to correct the problem is analogous to Applicant's "servicing the directory cache in response to testing dynamically restoring the storage unit in response to testing the storage device"; Applicant again respectfully disagrees with the Examiner's piecewise application of the art to the Applicant's claims.

Specifically, although the ECC circuit of Arimilli does try to correct errors in the data on the fly, as do most ECC type circuits, Applicant notes, the ECC circuit does not repair (i.e., service) the defective cache or portion thereof. To the contrary, it is well known that ECC circuits detect and/or correct the data that they operate on, depending on the class of error that is present. Furthermore, the retry and ECC circuits of Arimilli do not take the cache offline to perform their operations as recited in Applicant's claim 1.

Thus, Applicant submits Arimilli '511 clearly teaches away from Applicant's claimed invention, since Applicant's invention is directed toward taking the directory cache offline for testing during continued operation of the domain in response to detecting an uncorrectable error, requesting service of the directory cache, and returning the directory cache to an online status in response to the service.

Accordingly, for at least the reasons above, Applicant submits that the Examiner's rejection of claim 1 is in error and that claim 1, along with its dependent claims, patentably distinguishes over Arimilli '975 in view of Arimilli '511.

Applicant's independent claims 10 and 20 recite features that are similar to the features recited in claim 1. Thus, Applicant submits claims 10 and 20, along with their respective dependent claims, patentably distinguish over Arimilli '975 in view of Arimilli '511 for at least the reasons given above.

In light of the foregoing remarks, Applicant submits the application is in condition for allowance, and notice to that effect is respectfully requested. If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicant hereby petitions for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 501505/5681-55600/SJC.

Respectfully submitted,

Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8850

Date: October 6, 2005